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Citation: Appl. Phys. Lett. **96**, 073510 (2010); doi: 10.1063/1.3299014
View online: http://dx.doi.org/10.1063/1.3299014
View Table of Contents: http://aip.scitation.org/toc/apl/96/7
Published by the American Institute of Physics

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(Received 27 November 2009; accepted 4 January 2010; published online 19 February 2010)

The electric field perpendicular to the current flow is found to be significantly lower in junctionless transistors than in regular inversion-mode or accumulation-mode field-effect transistors. Since inversion channel mobility in metal-oxide-semionductor transistors is reduced by this electric field, the low field in junctionless transistor may give them an advantage in terms of current drive for nanometer-scale complementary metal-oxide semiconductor applications. This observation still applies when quantum confinement is present. © *2010 American Institute of Physics*.
[doi:10.1063/1.3299014]

The mobility of the carriers in a metal-oxide-silicon field-effect transistor (MOSFET) is strongly affected by the vertical electric field. The silicon universal mobility curves were published by Takagi *et al.* in 1994.[1,2] The universal mobility curves show that the electron mobility in the channel of a MOSFET transistor, μ, decreases as a function of the effective electric field, $\mathcal{E}$, following the law $\mu \approx \mathcal{E}^{-0.3}$. The study by Takagi *et al.* was limited to doping concentrations below 10^{18} cm^{-3} but a decrease in mobility with increasing electric field was observed for all cases of figure. As the dimensions of MOSFETs are scaled down, the effective oxide thickness (EOT) of the gate insulator is constantly decreased, which increases the vertical electrical field in the channel and increases carrier scattering, thereby decreasing mobility. It has been shown that electron channel mobility in MOSFETs has "historically" decreased from 400 to 300 and 130 $cm^2/V\,s$ when migrating from 0.8 to 0.6 and 0.13 μm technology nodes, respectively, making it necessary to develop strain silicon technology to keep switching speeds increasing with device size reduction.[3] Without strain technology, the channel mobility in modern MOSFETs would be equal or lower than that in heavily doped silicon (100 $cm^2/V\,s$ for electrons in N^+ silicon).[4]

Recently, a nanowire transistor called the "junctionless transistor" or the "gated resistor" has been introduced.[5,6] It is made of an N^+ (or P^+ for a p-channel device) doped silicon nanowire with a gate electrode. The doping concentration typically ranges between 10^{19} and 8×10^{19} cm^{-3}. Using a trigate device architecture it is possible to turn the device on and off and to obtain MOSFET-like electrical characteristics.[5,6] Even though the electrical characteristics of the junctionless transistor are similar to those of a regular MOSFET, there is a fundamental difference between the two devices. Classical MOSFETs, including multigate field-effect transistor, are normally-off devices, as the drain junction is reverse biased and blocks current flow if no channel is created between source and drain. To turn the device on, the gate voltage is increased in order to create an inversion channel. Since it is the electric field from the gate that attracts inversion carriers, the presence of a high electric field in the channel is inherent to the operation of inversion-mode MOSFETs. In accumulation-mode transistors, an accumulation channel is formed beneath the gate insulator because the carriers are attracted by the electric field from the gate.[7] As a result; accumulation-mode transistors suffer from the same field-induced mobility degradation as inversion-mode devices. The junctionless transistor, on the other hand, is basically a normally-on device where the work function difference between the gate electrode and the silicon nanowire shifts flatband voltage and threshold voltage to positive values (we consider here an n-channel device). When the device is turned on it is in flatband condition and, as a result, there is a zero electric field in the directions x and y perpendicular to the current flow direction. In other words, the electric field from the gate is used to deplete the device and turn it off. When the device is on, carriers flow from source to drain in a "channel" of neutral silicon, in which there is no electric field perpendicular to current flow.

As the cross section of the device is reduced below approximately 7 nm, confinement effects in the directions perpendicular to the current flow alter the electron concentration profile.[8,9] This raises the issue of calculating the electric field in nanowire devices. For instance, in a device that is in flatband conditions ($\mathcal{E}=0$) according to classical semiconductor device physics, the electric field is no longer equal to zero once quantum confinement effects are taken into consideration.[10] To calculate the electric field we use a two-dimensional Poisson–Schrödinger solver.[8]

Two n-channel devices are used for comparison as follows: an inversion-mode trigate MOSFET with a p-type channel doping concentration of 10^{17} cm^{-3} and a junctionless trigate MOSFET with an n-type channel doping concentration of 10^{19} cm^{-3}. Both devices have a silicon cross section of 5×5 nm^2 and an EOT of 1 nm. The buried oxide thickness is 10 nm and the back gate (substrate) is grounded. The gate voltage for the junctionless transistor (V_G) is chosen in such a way that the device is in "flatband" conditions (to be more accurate, V_G is chosen in such a way that the electron concentration, n, averaged over the device cross section, is equal to the doping concentration, or $(1/T_{Si}W_{Si})\int_0^{W_{Si}}\int_0^{T_{Si}} n(x,y)dxdy = N_D$, where T_{Si} is the silicon thickness, W_{Si} is the width of the nanowire, and N_D is the doping concentration). The gate voltage of the inversion-

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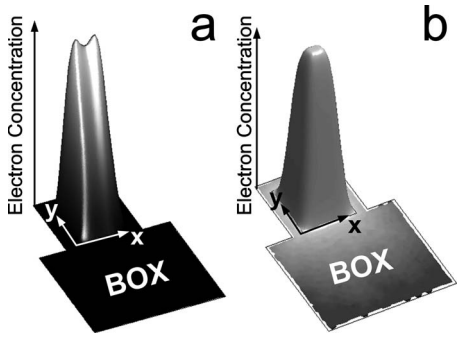

FIG. 1. Three-dimensional electron concentration profile in (a) an inversion-mode trigate MOSFET and (b) a heavily doped junctionless trigate MOSFET. $W_{Si}=T_{Si}=5$ nm; $T_{OX}=1$ nm. BOX is the buried oxide with thickness $T_{BOX}=10$ nm. In the inversion-mode device, $N_A=10^{17}$ cm^{-3}, the flatband voltage (V_{FB}) is -0.8 V and $V_G=V_{FB}+1.03$ V. In the junctionless device, $N_D=10^{19}$ cm^{-3}, $V_{FB}=0.8$ V, and $V_G=V_{FB}$.

mode device is chosen in such a way that the electron concentration, $n(x,y)$, integrated over the device cross section, is equal to that in the junctionless device. Thus, if mobility was constant and equal in both devices, they would carry exactly the same drain current. Figure 1 shows a three-dimensional view of the electron concentration profile in the two devices. Both devices have a peak concentration of approximately 1.6×10^{19} cm^{-3}. Figure 2 shows the electron concentration in the form of isoconcentration contour lines, superimposed to a grayscale representation of the norm of the electric field. The lower the field, the darker the gray shading, and the higher the field the lighter the gray shading. Some particular values of the field are given at locations marked by the symbol "⊗." In the inversion-mode device, the majority of the inversion carriers, and in particular the points of peak electron concentration, are located in high electric field regions. This is quite normal, considering that inversion electrons are present because they are attracted by the electric field emanating from the gate. Accumulation-mode devices show results that are basically identical to those of inversion-mode devices. In the junctionless transistors, on the other hand, the

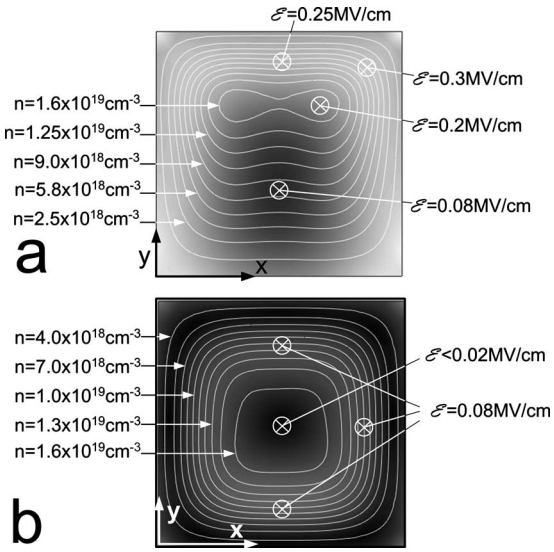

FIG. 2. Electron concentration contour lines superimposed to a grayscale representation of the amplitude of the electric field. The lower the field, the darker the gray shading, and the higher the field the lighter the gray shading. Field values are given at locations marked by the symbol "⊗." (a) Inversion-mode device and (b) junctionless device. Same parameters as in Fig. 1.

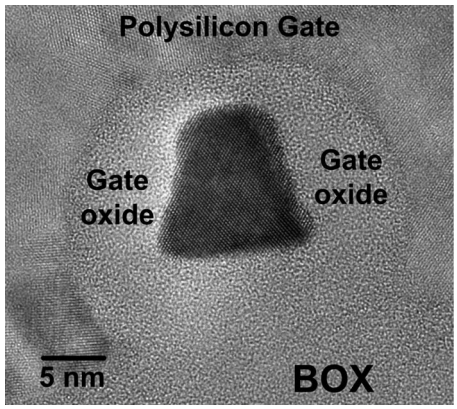

FIG. 3. Transmission electron microscope photograph of a junctionless nanowire transistor.

peak electron concentration coincides with the region of lowest electric field. The field is not quite equal to zero but it is much lower ($\mathcal{E}<0.02$ MV/cm) than in the inversion-mode device ($\mathcal{E}\geq0.2$ mV/cm). This may offer an advantage to junctionless transistors in terms of current drive, once device size reaches the nanoscale level.

Both inversion-mode and junctionless devices were fabricated using the process described in Ref. 5. The channel length is 1 μm, the gate oxide thickness is 5 nm and the doping concentration is 10^{17} cm^{-3} (N_A) and 10^{19} cm^{-3} (N_D) in the inversion-mode and junctionless FETs, respectively. The cross section of a junctionless device is shown in Fig. 3. Figure 4 shows the normalized transconductance, g_m/g_{mmax} in the two types of devices as a function of gate voltage. The transconductance was measured at low drain voltage (50 mV), and is, therefore, proportional to the electron mobility. Both devices have a threshold voltage, V_{TH}, of approximately 0.7 V. As gate voltage is increased beyond V_{TH}, the mobility in the inversion-mode device reaches a peak and then decreases rapidly because of the high electric field in the channel. In the junctionless transistor, the decrease in mobility with gate voltage is much less pronounced, as a result of the lower electric field perpendicular to the current flow. The peak mobility in the junctionless is difficult to estimate from measurements. The simple resistor equation $I_D=q\mu N_D(T_{Si}W_{Si}/L)V_{DS}$ is valid in flatband only, i.e., for a gate voltage significantly higher than that at which the peak of transconductance occurs. It is also difficult to measure the mobility in the regular trigate device because the gate oxide thickness varies with the crystal orientation of the different sides of the nanowire (Fig. 3). From comparison between

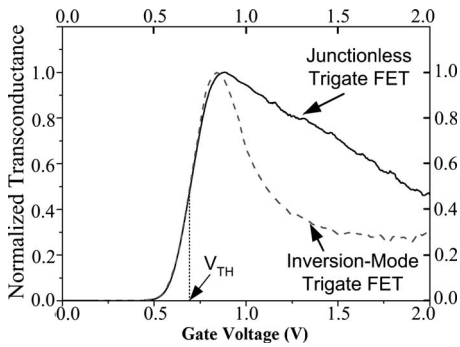

FIG. 4. Normalized transconductance g_m/g_{mmax} vs gate voltage in inversion-mode and junctionless trigate nanowire transistors.

measurements simulation results, however, we estimate that the mobility in the junctionless device is approximately 80 $cm^2/V\ s$ when the device is turned on.

Doping fluctuations are a concern for devices with small dimensions. For example considering $T_{Si}=W_{Si}=10$ nm and a gate length of 20 nm, the statistical number of doping atoms in the channel region is 0.002, 2, and 20 for doping concentrations of 10^{15}, 10^{18}, and 10^{19} cm^{-3}. "Undoped" devices have a typical doping concentration of 10^{19} cm^{-3} which means that, statistically, every device in 500 will contain a doping atom and, therefore, have a threshold voltage different from that of the other devices. In a moderately doped device ($N_A=10^{18}$ cm^{-3}), there is an average of two doping atoms in the channel. In practice, many devices will have one or three doping atoms, which has a significant impact on variability. In a heavily doped junctionless device ($N_D=10^{19}$ cm^{-3}), the average number of doping atoms is 20. This relatively large number should render junctionless devices less sensitive to doping impurity fluctuation problems than other types of MOSFETs.

In conclusion, we observe that, in inversion-mode and accumulation mode trigate nanowire MOSFETs, the peak electron concentration coincides with the presence high electric fields, while the opposite is seen in heavily doped junctionless transistors. Since high electric fields are known to reduce mobility, this gives an advantage to junctionless devices in terms of current drive.

This work is supported by the Science Foundation Ireland Grant No. 05/IN/I888: Advanced Scalable Silicon-on-Insulator Devices for Beyond-End-of-Roadmap Semiconductors. This work has also been enabled by the Programme for Research in Third-Level Institutions. This work was supported in part by the European Community (EC) Seventh Framework Program through the Networks of Excellence NANOSIL and EUROSOI+under Contract Nos. 216171 and 216373. The authors also wish to thank Dr. N. Petkov for taking the TEM picture.

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